IN THE CLAIMS

Kindly amend claim 1 as shown in the following claim listing:

1. (currently amended) A leading edge blanking circuit comprising:

an input terminal for receiving a trigger signal indicating a time at which a blanking period should commence;

switching means arranged to be activated by the trigger signal to change from a first state to a second state;

comparison means having a first input terminal being connected to a reference source, a second input terminal arranged to receive a voltage which ramps over time in response to the trigger signal and an output terminal for providing an output signal of the leading edge blanking circuit which changes state subsequent to the voltage at the second terminal of the comparison means reaching the voltage level supplied by the reference source to the first terminal; and

a charging circuit for providing the ramp voltage to the second input terminal of the comparison means,

the circuit being characterised in that the time taken for the ramp voltage to reach the voltage level supplied by the reference source is ~~variable and dependent upon~~ deliberately

adjusted as a function of a control signal received at a control input of the circuit.

2. (original) The leading edge blanking circuit of claim 1, wherein the reference voltage supplied to the first terminal of the comparison means comprises the control signal.

3. (original) The leading edge blanking circuit of claim 2, wherein the charging circuit comprises a current source and a capacitor, the current source being arranged to charge the capacitor following an initiation of change in state of the switching means from the first state to the second state and, wherein, the voltage supplied to the second input terminal of the comparison means is arranged to ramp in accordance with a charged state of the capacitor.

4. (original) The leading edge blanking circuit of claim 1, wherein the switching means comprises a transistor switch, the charging circuit comprises a capacitor connected in parallel with the transistor switch and a current source arranged to charge the capacitor when the transistor switch is not in the first state, the comparison means comprises a comparator, wherein the first terminal is a non-inverting input and the second terminal is an

inverting input, the first terminal being connected to the control signal and the second terminal being connected to a terminal of the charging circuit at a point between the current source and the capacitor.

5. (original) The leading edge blanking circuit of claim 1, wherein the reference voltage supplied to the first terminal of the comparison means is a fixed voltage reference source and, wherein, the control signal is arranged to vary a current level in the charging circuit, to change the rate at which the voltage at the second input terminal of the comparison means ramps over time.

6. (original) The leading edge blanking circuit of claim 5, wherein the charging circuit comprises a voltage source, a transistor and a capacitor, the transistor being responsive to the voltage source and the control signal to turn on and to supply a charging current to the capacitor.

7. (original) The leading edge blanking circuit of claim 6, wherein the charging current to the capacitor is a variable current, dependent upon a potential difference between the voltage source and the control signal.

8. (original) The leading edge blanking circuit of claim 1, wherein:

the first switching means comprises a transistor switch;

the comparison means comprises a comparator in which the first terminal comprises a non-inverting terminal connected to a fixed voltage reference source, and the second input terminal comprises an inverting input; and

the charging circuit comprises a capacitor, transistor and a voltage source, the capacitor being connected in parallel with the first switching means and having one terminal thereof connected in common to the inverting input of the comparator and an output terminal of the transistor, the transistor being arranged to supply a variable current from the voltage source dependent upon a voltage level of the control signal supplied to its control input.

9. (previously presented) A power controller for a switched mode power supply for supplying a control signal to a leading edge blanking circuit of claim 1, the power controller being arranged to output the control signal at a substantially constant level during a first operating power range of the SMPS and, in a second operating power range to progressively decrease the level of the control signal as the output power requirements of the SMPS decrease.

10. (original) A power controller according to claim 9, wherein the first range of operating power range comprises a normal operating power range of the SMPS being controlled, and the second range comprises a low power to very low power operating range.

11. (original) A power controller according to claim 9, wherein the power controller comprises an amplifier, a transistor, a supply voltage, a variable voltage source whose voltage depends upon the power output requirements of the SMPS, a voltage reference source, and a control output terminal for supplying the control signal "Timer Level", the control output terminal being connected to the supply voltage via a first biasing means and to one terminal of the transistor, the voltage reference source being connected to a non-inverting input of the amplifier, an inverting input of the amplifier being connected via second biasing means to the variable voltage source and directly to another terminal of the transistor, and an output of the amplifier being arranged to operate and progressively increase a control current input to the transistor so as to progressively turn on the transistor during the second operating range and being further arranged to turn off the transistor during the first, normal, operating range, wherein when the transistor is turned off, the voltage of the Timer Level

control signal is at a maximum constant value and, when the transistor is in a linearly operating state the voltage of the Timer Level control signal is arranged to decrease as the transistor progressively turns on.

12. (original) A power controller as claimed in claim 9, wherein the power controller comprises an amplifier, a transistor, a supply voltage, a voltage reference source, a variable voltage source whose voltage level is dependent upon the output power requirements of the SMPS and first and second bias resistors, wherein: the voltage reference source is connected between a lower rail voltage and a non-inverting input of the amplifier, the power supply is connected between the lower rail voltage and a first terminal of the first bias resistor to provide an upper rail voltage thereto, the variable voltage source is connected between the lower rail voltage and a common connection between a first terminal of the second bias resistor and a first output terminal of the power controller to provide a power level control signal "Trip Level" to the said first output terminal, an inverting input of the amplifier is commonly connected to a second terminal of the second bias resistor and a third terminal of the transistor, an output terminal of the amplifier is connected to a first terminal of the transistor and wherein a second terminal of the transistor is connected in

common to a second output terminal of the power controller and a second terminal of the first bias resistor and to provide the control signal "Timer Level" to the said second output terminal.

13. (previously presented) A switch mode power supply including a flyback converter comprising a power controller arranged to set a desired power output of the SMPS by generating a control signal "trip level" at which the SMPS is to revert from an on-power state to an off-power state, a switch controller for controlling a main switching component of the SMPS in accordance with the power requirements as set by the "trip level" signal and a leading edge blanking circuit for providing an output signal "blank" arranged to validate or inhibit resetting of the switch controller, wherein the leading edge blanking circuit comprises a leading edge blanking circuit according to claim 1.

14. (original) An SMPS according to claim 13, wherein the power controller is arranged to supply the "timer level" signal to the leading edge blanking circuit such that at trip levels above a particular threshold, the "timer level" is a substantially constant voltage regardless of the actual "trip level" and that the "timer level" is arranged to decrease once the "trip level" decreases below the threshold level.

15. (original) A method of controlling a leading edge blanking circuit of the type in which, conventionally, a leading edge blanking time is fixed, the method comprising, during a normal power operating range of a switch mode power supply of which the leading edge blanking circuit forms a part, providing a substantially constant reference voltage to a voltage controlled switch of the leading edge blanking circuit so as to maintain the leading edge blanking period to be of a constant time period and being characterised in that, in a low to very low operating power range of the SMPS, a reduced level reference voltage is provided to the voltage controlled switch of the leading edge blanking circuit to adaptively reduce the leading edge blanking period.